Plan 9 is offering a Power Line Communications (PLC) Narrow Band (0-500kHz) Receiver IP Programmable Gain Amplifiers (PGAs) designed with low noise and outstanding linearity and MTPR (Multi-Tone Power Ratio) performance receiving OFDM signals.

Applications include:

- *All PLC related standards*
- *Smart power meter communications*
- *Smart House controls*
- *Industrial Internet of Things*

Features of this Receiver IP:

- *18 Vpp input capability*
- *>500KHz Full Power Bandwidth*
- *Single ended Operation*
- *Switchable power down mode*
- *Six-bit Programmable gain of +48 dB to -21 dB*
- *<2.7mA idle current typical*
- *VDD range is 5V to 3V (3.3 V typical)*
- *RX IP total area is less than 0.160 mm^2*

Description

The AC power line was not designed for data transmission. High voltage, current spikes, induced noise, switching noise, low impedance loads, lossy transmission, etc., all challenge a communication channel and the frontline AFE components. The Plan 9 receiver IP is designed with some of these challenges in mind.

The PGA amplifier is designed to provide high MTPR performance (typical 69-91 dB, over the gain range) at the highest output signal swings of 2.3 Vpp and the highest PLC frequency of 500kHz.

The amplifier saturation characteristics allow it to track the zero crossover without distortion when the amplitude of the signal exceeds the PGA dynamic range. This gain range combined with extended voltage range ESD for PGA1 allows the signal processing circuitry to determine the zero crossover accurately and make accurate gain corrections for a broad range of input signals.

Three bits are used with a 3 to 8 decoder to program PGA1 gain settings from -18 dB to +24 dB in 6 dB steps. Three bits are used with a 3 to 8 decoder to program PGA2 from +24 dB to -3 dB. PGA2 gain steps are +24 dB, +9 dB, +6 dB, +3 dB, +1 dB, 0 dB, -1 dB and -3 dB. This combination of gain steps allows fine gain adjustment for a wide range of signals. The additional 24 dB step allows for higher gain of lower level signals that may be transmitted from a greater distance.

PGA1 and PGA2 are optimized to reduce 1/f noise to allow good SNR across the entire PLC band.

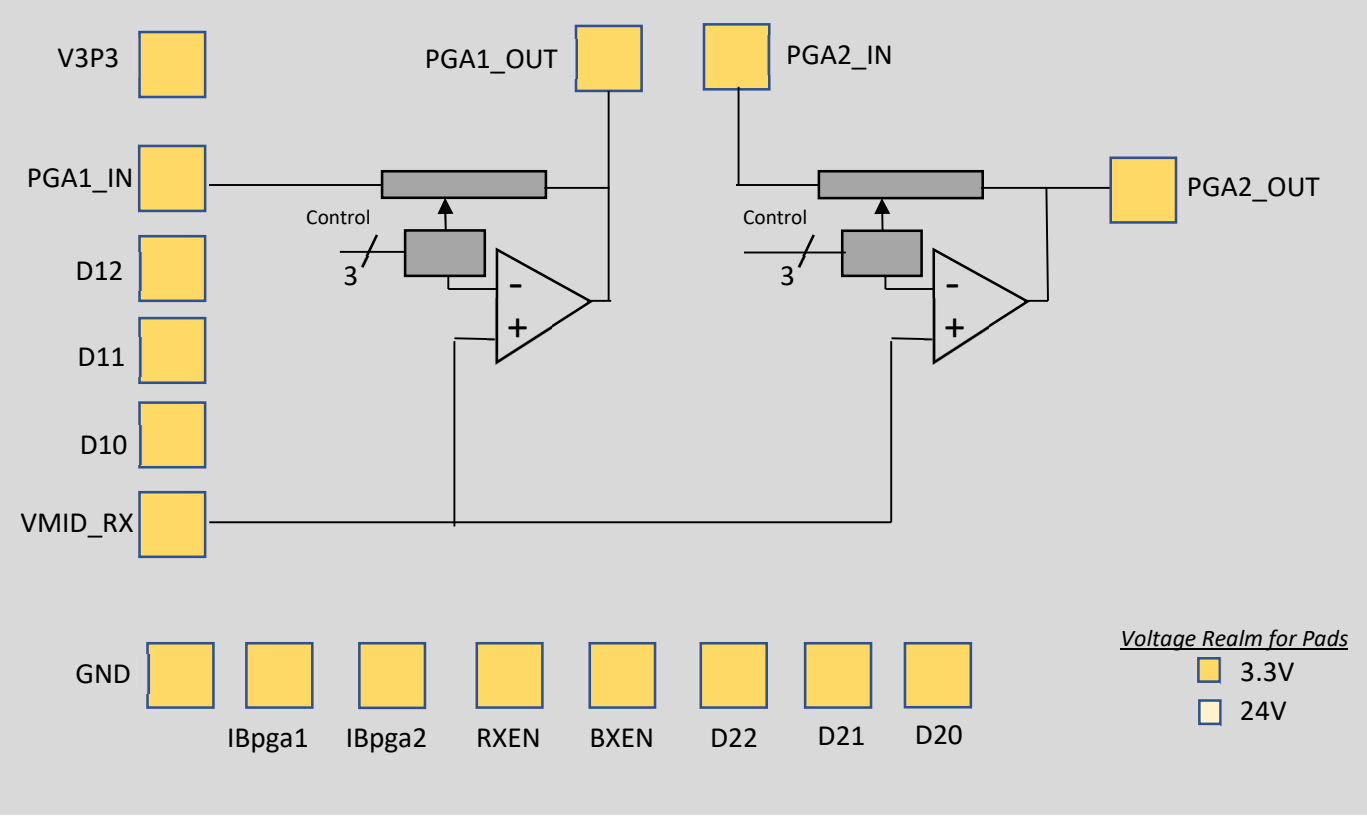
The output of PGA1 and input of PGA2 are brought off-chip to provide a low frequency coupling capacitor. A passive filter can be inserted between PGA1 and PGA2.

Availability

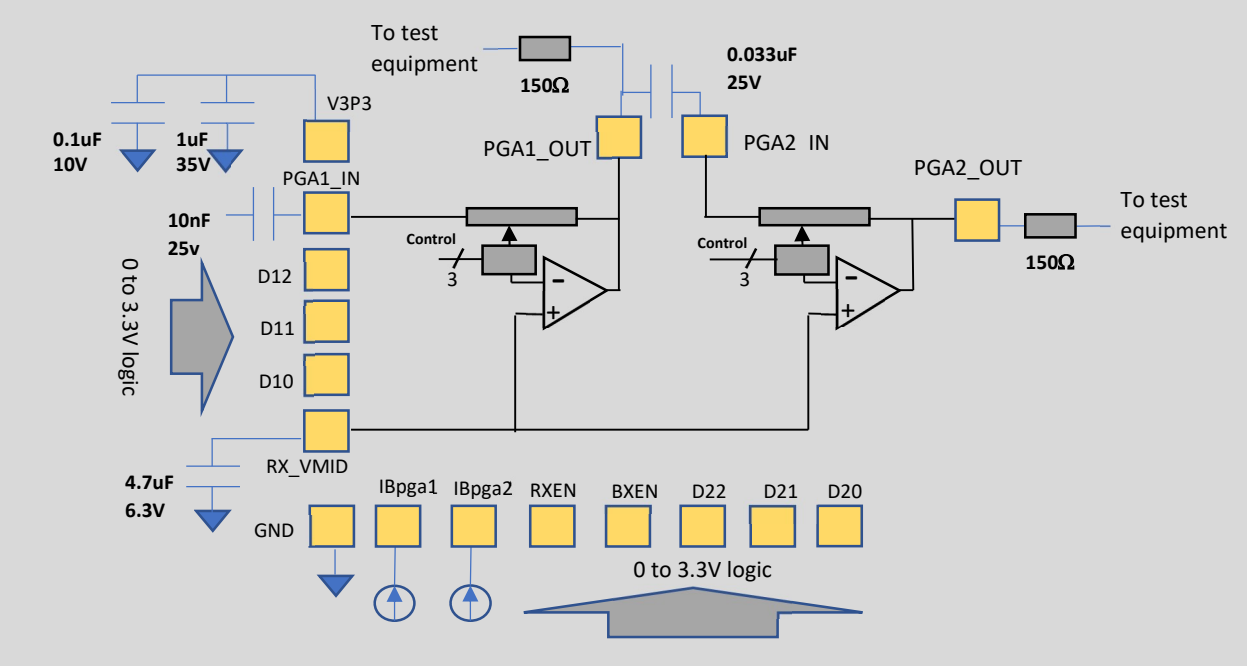
Additional information and demos are available with restrictions. Email: info@plan9inc.com

The IP ownership is offered for sale.

Block Diagram



Application Circuit



Pin Description

Pin Name	Pin on Package	ESD Requirements	Description
PGA1_IN	23	9.5V	PGA1 Input, Extended Voltage range
D12	32	5V	PGA1 control bit (MSB)
D11	1	5V	PGA1 control bit
D10	2	5V	PGA1 control bit (LSB)
RX_VMID	25	5V	V3p3/2 bias voltage
GND	Paddle	none	Down bonded to package paddle
IBIAS PGA1	Internal	5V	Low variation bias current
IBIAS PGA2	Internal	5V	Low variation bias current
RXEN	22	5V	Active Receiver from standby, H-active
BXEN	28	5V	Active Bias from off, H-active
D22	29	5V	PGA2 control bit (MSB)
D21	30	5V	PGA2 control bit
D20	31	5V	PGA2 control bit (LSB)
PGA2_OUT	17	5V	PGA2 Output
PGA2_IN	20	5v	PGA2 Input
PGA1_OUT	21	5V	PGA1 Output
V3p3	24	5V	Receiver Supply voltage typically 3.3 V ±10%

Three bits are used to program the PGA1 to gain settings from -18 dB to +24 dB in 6 dB steps. There is a power down state that allows PGA1 to be powered down when not in use allowing a low-power state for TX or RX.

A 3 to 8 Decoder is used in conjunction with gain setting switches in the block to set the gain through the ±18 dB range and control power down. The truth table for the decoder is shown below

Description	Data Bits			
	D12	D11	D10	PGA1 Gain
-18 dB gain	0	0	0	-18 dB
-12 dB gain	0	0	1	-12 dB
-6 dB gain	0	1	0	-6 dB
0 dB gain	0	1	1	0 dB
6 dB gain	1	0	0	6 dB
12 dB gain	1	0	1	12 dB
18 dB gain	1	1	0	18 dB
24 dB gain	1	1	1	24 dB

Three bits are used to program the PGA2 to gain settings from -3 dB to +24 dB in 6 dB steps. There is a power down state that allows PGA2 to be powered down when not in use allowing a low-power state for TX or RX.

A 3 to 8 Decoder is used in conjunction with gain setting switches in the block to set the gain through the ±18 dB range and control power down. The truth table for the decoder is shown below:

Description	Data Bits			
	D22	D21	D20	PGA2 Gain
-3 dB gain	0	0	0	-3 dB
-1 dB gain	0	0	1	-1 dB
0 dB gain	0	1	0	0 dB
1 dB gain	0	1	1	1 dB
3 dB gain	1	0	0	3 dB
6 dB gain	1	0	1	6 dB
9 dB gain	1	1	0	9 dB
24 dB gain	1	1	1	24 dB

Specifications

Simulation results are included to show how well the silicon matches simulation. Agreement between measured and simulated values validates the simulations and that layout minimally impacts the design. Thus, with good agreement, simulations over the corners can be more relied upon to help predict long term manufacturing performance limits.
Below are the Overall Conditions for testing, except where noted. The Receiver was tested over combinations of voltage, temperature, and process corner. In addition, Monte Carlo analysis was employed for certain tests.

Corners used are Typ., FF, SS, FS, SF with various combinations of resistor and capacitor corners.
VDD = 10V and 24V (tested at extreme range, see recommendations)
V3P3 = 3V,3.3V and 3.6V
Junction Temperature = -40C, 27C, and 150C
Rload= 1M Ω (resistive load)
Cload= 20pF

Absolute Max

Symbol	Description	Conditions	Min	Typ	Max	Units
	V3P3 Supply Range		-0.4		5.5	V
	Control pins- D1N, D2N, RXEN, BXEN		-0.4		5.5	V
	PGA1_OUT, PGA2_OUT		-0.4		5.5	V
	Junction Temperature		-40		150	C

Recommended

Symbol	Description	Conditions	Min	Typ	Max	Units
	VDD		10		22	V
	V3P3 Supply Range		3		3.6	V
	Junction Temperature		-40		135	C

Power Supply Voltages and Currents

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	V3P3 Supply Range		3	3.3	3.6	3	3.3	3.6	V
	RX V3p3 Active Current	No signal (includes Plan 9 bias)	1.71	2.6	4.85		2.04		mA
	RX V3P3 Powered Down Current	PGA1+PGA2	7.5		255				nA

PGA1 Inputs

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Input Nominal			V3p3/2			V3p3/2		V
	Input Range (single ended)	AC coupled input	(0.5-V3p3/2)/gain		((V3p3/2)-0.5)/gain	-9		9	V
	Input offset Voltage	Input referred	-5		5		1.5		mV
	PGA1 Input Resistance	Gain=-18 dB		5.4			5.75		kΩ
		Gain=-12 dB		5.76			5.95		kΩ
		Gain=-6 dB		6.7			6.86		kΩ
		Gain=0 dB		9.99			10.1		kΩ
		Gain=6 dB		12.96			13.04		kΩ
		Gain=12 to 24 dB		14			14.7		kΩ

PGA1 Output

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Active Output Nominal			V3p3/2			V3p3/2		V
	Linear Output Range		0.5		V3p3-0.5	0.5		V3p3-0.5	V
	Slew Rate	20pF, 1M Ohm load							
		Gain=-18 to 18 dB		20			20		V/µS
		Gain=24 dB		14.38			14.25		V/µS

PGA1 Gain, Bandwidth

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	-18 dB Gain	20pF, 1M Ohm load		-18			-17.96		dB
	-12 dB gain			-12			-11.95		dB
	-6 dB gain			-6			-5.93		dB
	0 dB gain			0			-0.01		dB
	6 dB gain			6			5.9		dB
	12 dB gain			12			11.88		dB
	18 dB gain			18			17.92		dB
	24 dB gain			24			24.17		dB
	Gain Step			6			6.04		dB
	Gain Error		-2		2		1		%
	Gain Error Drift		-6.5		6.5				ppm/C
	PGA1 Bandwidth (3 dB)	-18 dB gain, 20 pF,1MΩ		23			25.24		MHz
		-12 dB gain, 20 pF,1MΩ		24			25.58		MHz
		-6 dB gain, 20 pF,1MΩ		26.5			27		MHz
		0 dB gain, 20 pF,1MΩ		27			27		MHz
		6 dB gain, 20 pF,1MΩ		10			12.98		MHz
		12 dB gain, 20 pF,1MΩ		6.3			6.96		MHz
		18 dB gain, 20 pF,1MΩ		4.2			4.42		MHz
		24 dB gain, 20 pF,1MΩ		2.3			2.66		MHz
	Full Power Bandwidth	VO=2.3 Vpp, 24 dB gain,20 pF,1MΩ	500						kHz

PGA1 Sensitivity/Noise, PSRR

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	PLC Band	24 dB gain 35-500 kHz		19			20.53		µV rms
	CEN-A (Integrated noise input ref)	24 dB gain 35kHz to 95kHz		6.93			7.38		µV rms
	CEN-B (integrated noise input ref)	24 dB gain 95k to 125kHz		5.88			5.22		µV rms
	CEN-C (integrated noise input ref)	24 dB gain 125kHz to 140kHz		4.16			3.69		µV rms
	CEN-D (integrated noise input ref)	24 dB gain 140kHz to 148kHz		2			2.69		µV rms
	ARIB Std-T84 (input noise ref)	24 dB gain 35kHz to 420kHz		18			18.7		µV rms
	FCC-low (integrated noise input ref)	24 dB gain 35kHz to 125kHz		8.83			9		µV rms
	FCC-G3 (integrated noise input ref)	24 dB gain 150kHz to 490kHz		17			17.6		µV rms
	PSRR (V3p3) Input ref	500 Ohm load, @50kHz		50					dB

PGA1 Distortion

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	2nd Harmonic (Over gain range)	Vout=2.3Vpp Freq=250kHz	-85		-52		-61		dB
	3rd Harmonic (Over gain range)	Vout=2.3Vpp Freq=250kHz	-90		-52		-85		dB
	MTPR Average Bin/Peak Bin	2.3Vpp, CF=4, 260 tones (appx 9k to 480kHz) Fund freq=488.28125Hz	55/51		95/77				dB
		-18 dB Gain, 20 pF,1MΩ					80/63.3		dB
		-12 dB Gain, 20 pF,1MΩ					87/71.4		dB
		-6 dB Gain, 20 pF,1MΩ					91/77.5		dB
		0 dB Gain, 20 pF,1MΩ					91/77.7		dB
		6 dB Gain, 20 pF,1MΩ					91/76.7		dB
		12 dB Gain, 20 pF,1MΩ					91/75		dB
		18 dB Gain, 20 pF,1MΩ					75/60		dB
		24 dB Gain, 20 pF,1MΩ					69/54		dB

PGA2

PGA2 Inputs

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Input Nominal			V3p3/2			V3p3/2		V
	Input Range (single ended)	AC coupled input	(0.5-V3p3/2)/gain		((V3p3/2)-0.5)/gain	-1.626		1.626	V
	Input offset Voltage	Input referred	-5		5		0.7		mV
	PGA2 Input Resistance	Gain=-3 dB		5.82			6.02		kΩ
		Gain=-1 dB		5.28			5.44		kΩ
		Gain=-0 dB		4.99			5.15		kΩ
		Gain=1 dB		4.7			4.86		kΩ
		Gain=3 dB		4.14			4.29		kΩ
		Gain=6 dB		3.33			3.47		kΩ
		Gain=9 dB		2.61			2.76		kΩ
		Gain=24 dB		0.593			0.734		kΩ

PGA2 Output

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Active Output Nominal			V3p3/2			V3p3/2		V
	Linear Output Range		0.5		V3p3-0.5	0.5		V3p3-0.5	V
	Slew Rate	20pF, 1M Ohm load All Gain Settings		23			23		V/µS

PGA2 Gain, Bandwidth

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	-18 dB Gain	20pF, 1M Ohm load		-3			-2.9		dB
	-12 dB gain			-1			-0.9		dB
	-6 dB gain			0			0.09		dB
	0 dB gain			1			1.09		dB
	6 dB gain			3			3.04		dB
	12 dB gain			6			6.03		dB
	18 dB gain			9			9.02		dB
	24 dB gain			24			23.9		dB
	Gain Step		1	3	14	1	3	14	dB
	Gain Error		-2		2		1		%
	Gain Error Drift		-6.5		6.5				ppm/C
	PGA2 Bandwidth (3 dB)	-3 dB gain, 20 pF,1MΩ		15.9			32.5		MHz
		-1 dB gain, 20 pF,1MΩ		16.6			30.12		MHz
		0 dB gain, 20 pF,1MΩ		17			30.21		MHz
		1 dB gain, 20 pF,1MΩ		17.4			29.7		MHz
		3 dB gain, 20 pF,1MΩ		17.5			25		MHz
		6 dB gain, 20 pF,1MΩ		16.75			22		MHz
		9 dB gain, 20 pF,1MΩ		14.5			18.8		MHz
		24 dB gain, 20 pF,1MΩ		5.8			5.14		MHz
	Full Power Bandwidth	2.3 Vpp,24 dB gain,20 pF,1MΩ	500						kHz

PGA2 Sensitivity/Noise, PSRR

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	PLC Band	24 dB gain 35-500 kHz		5.28			5.21		µVrms
	CEN-A (Integrated noise input ref)	24 dB gain 35kHz to 95kHz		1.86			1.721		µVrms
	CEN-B (integrated noise input ref)	24 dB gain 95k to 125kHz		1.56			1.226		µVrms
	CEN-C (integrated noise input ref)	24 dB gain 125kHz to 140kHz		1.103			0.867		µVrms
	CEN-D (integrated noise input ref)	24 dB gain 140kHz to 148kHz		0.75			0.633		µVrms
	ARIB Std-T84 (input noise ref)	24 dB gain 35kHz to 420kHz		4.8			4.39		µVrms
	FCC-low (integrated noise input ref)	24 dB gain 35kHz to 125kHz		2.36			2.123		µVrms
	FCC-G3 (integrated noise input ref)	24 dB gain 150kHz to 490kHz		4.49			4.128		µVrms
	PSRR (V3p3) Input ref	500 Ohm load, @50kHz		50					dB

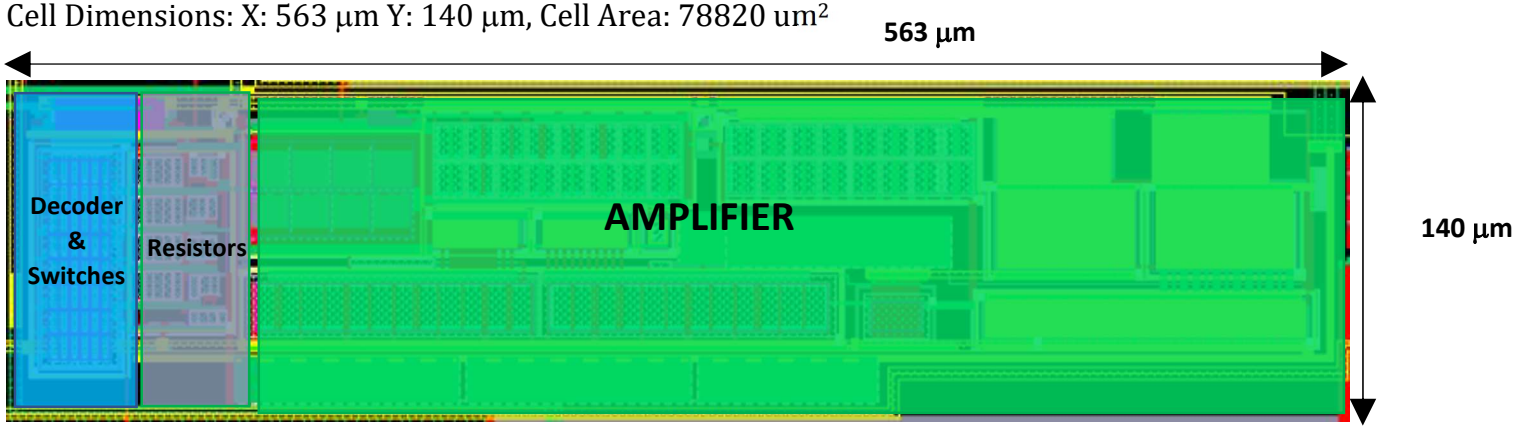
PGA2 Distortion

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	2nd Harmonic (Over gain range)	Vout=2.3Vpp Freq=250kHz	-95		-60		-88		dB
	3rd Harmonic (Over gain range)	Vout=2.3Vpp Freq=250kHz	-95		-60		-89		dB
	MTPR Average Bin/Peak Bin	2.3Vpp, CF=4, 260 tones (appx 9k to 480kHz) Fund freq=488.28125Hz	55/54		95/79				dB
		-3 dB Gain, 20 pF,1MΩ					91/76.9		dB
		-1 dB Gain, 20 pF,1MΩ					91/78		dB
		0 dB Gain, 20 pF,1MΩ					91/78		dB
		1 dB Gain, 20 pF,1MΩ					91/77.7		dB
		3 dB Gain, 20 pF,1MΩ					92/79		dB
		6 dB Gain, 20 pF,1MΩ					92/76.9		dB
		9 dB Gain, 20 pF,1MΩ					92/76.8		dB
		24 dB Gain, 20 pF,1MΩ					82/64		dB

Physical

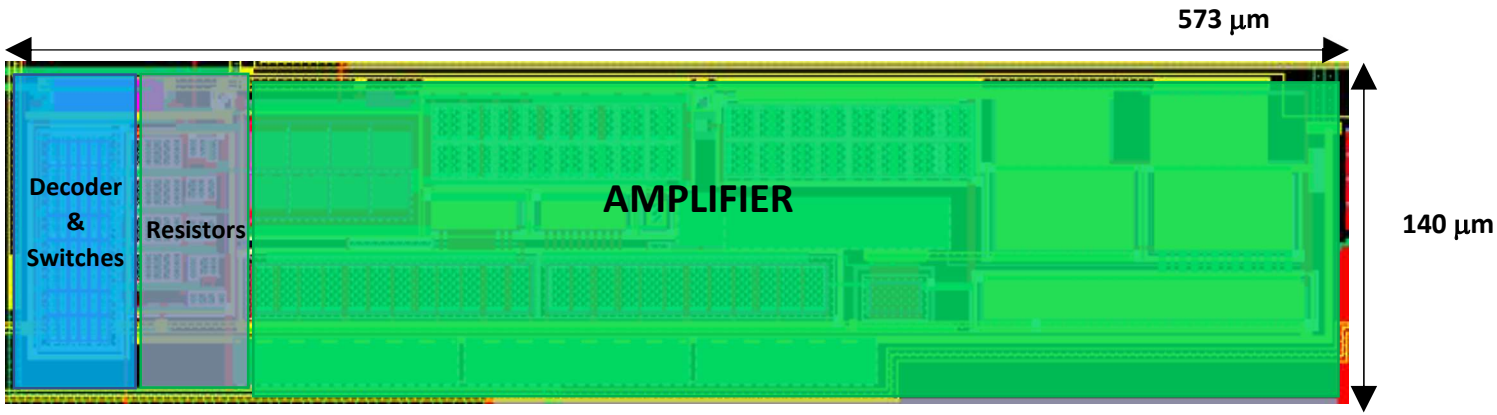
PGA1 (W/O bond pads)

Cell Dimensions: X: 563 µm Y: 140 µm, Cell Area: 78820 um^2



PGA2 (W/O Bond pads)

Cell Dimensions: X: 573 µm Y: 140 µm, Cell Area: 80220 um^2

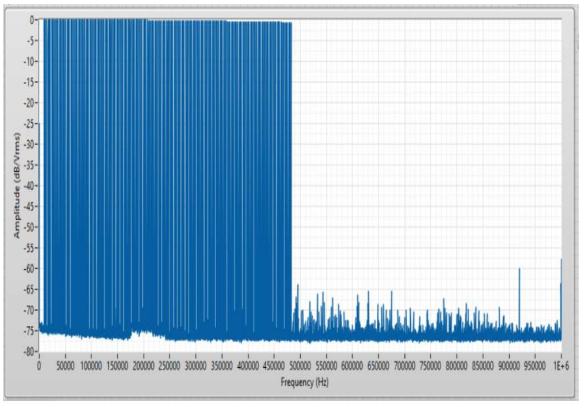


Measurement Results

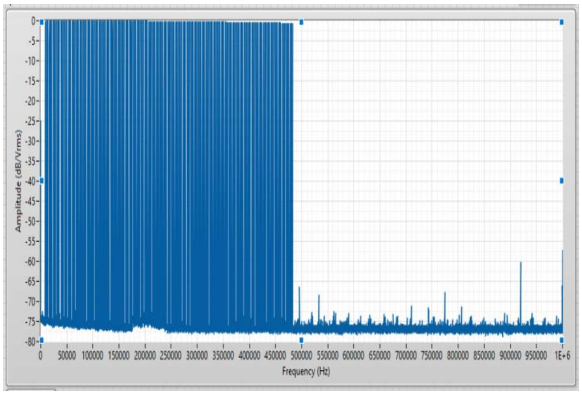
MTPR

Typical measurement result of MTPR signal with over 200 tones producing peaks of 1.15 V with VDD= 3.3V, for PGA1 and PGA2 is shown below. This measurement uses tones and empty bins evenly spaced. Intermodulation distortion collects in the empty bins and is compared to the signal, with both an average MTPR S/N and a worst-case bin calculation. All dB calculations are in Volts.

PGA1, Gain=12 dB
Each tone: -42.42 dB, **Worst MTPR:** 70.74 dB,
Avg MTPR: 87.35 dB

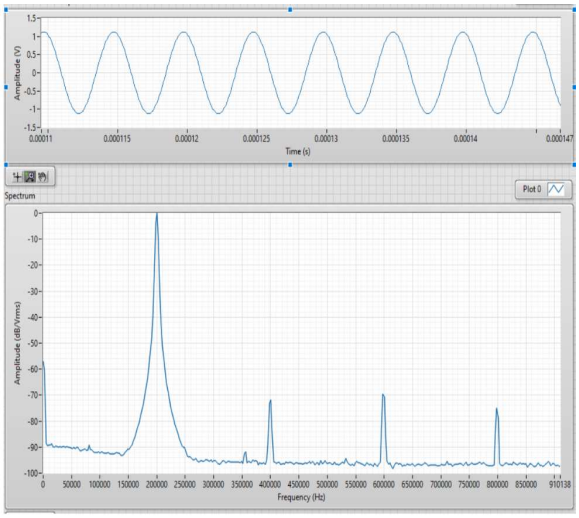


PGA2, Gain=9 dB
Each tone: -42.42 dB, **Worst MTPR:** 76.7 dB,
Avg MTPR: 92.8 dB

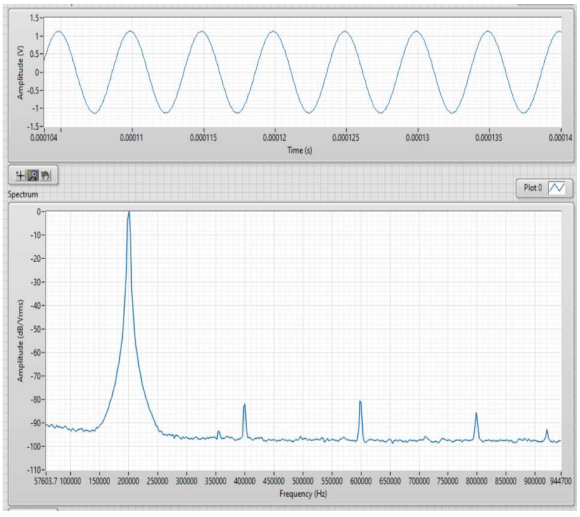


HARMONIC DISTORTION

PGA1, Gain=12 dB
Vout = 2.3 Vpp, Load= 1M Ω, VDD=3.3V
2nd Harmonic: -70dB 3rd Harmonic: -69dB

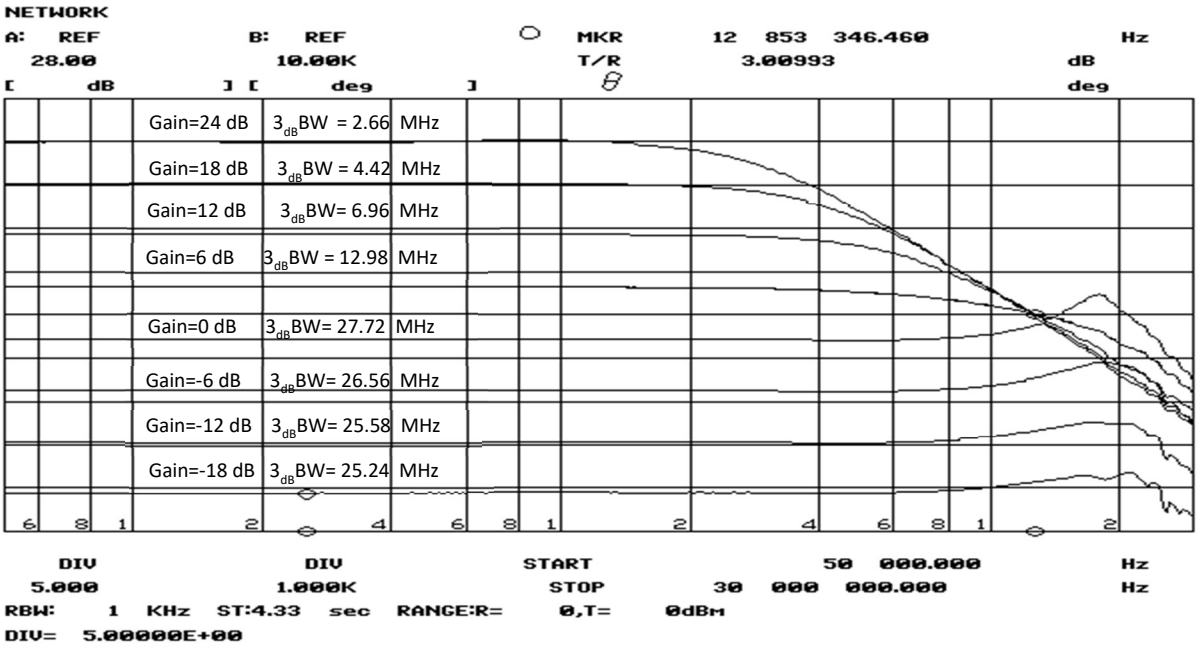


PGA2, Gain=9dB
Vout = 2.3 Vpp, Load= 1M Ω, VDD=3.3V
2nd Harmonic: -81 to -84dB 3rd Harmonic: -79.6 dB



Bode Plot

PGA1, All gain settings, Load= 1M Ω, VDD=3.3V



PGA2, All gain settings, Load= 1M Ω VDD=3.3V