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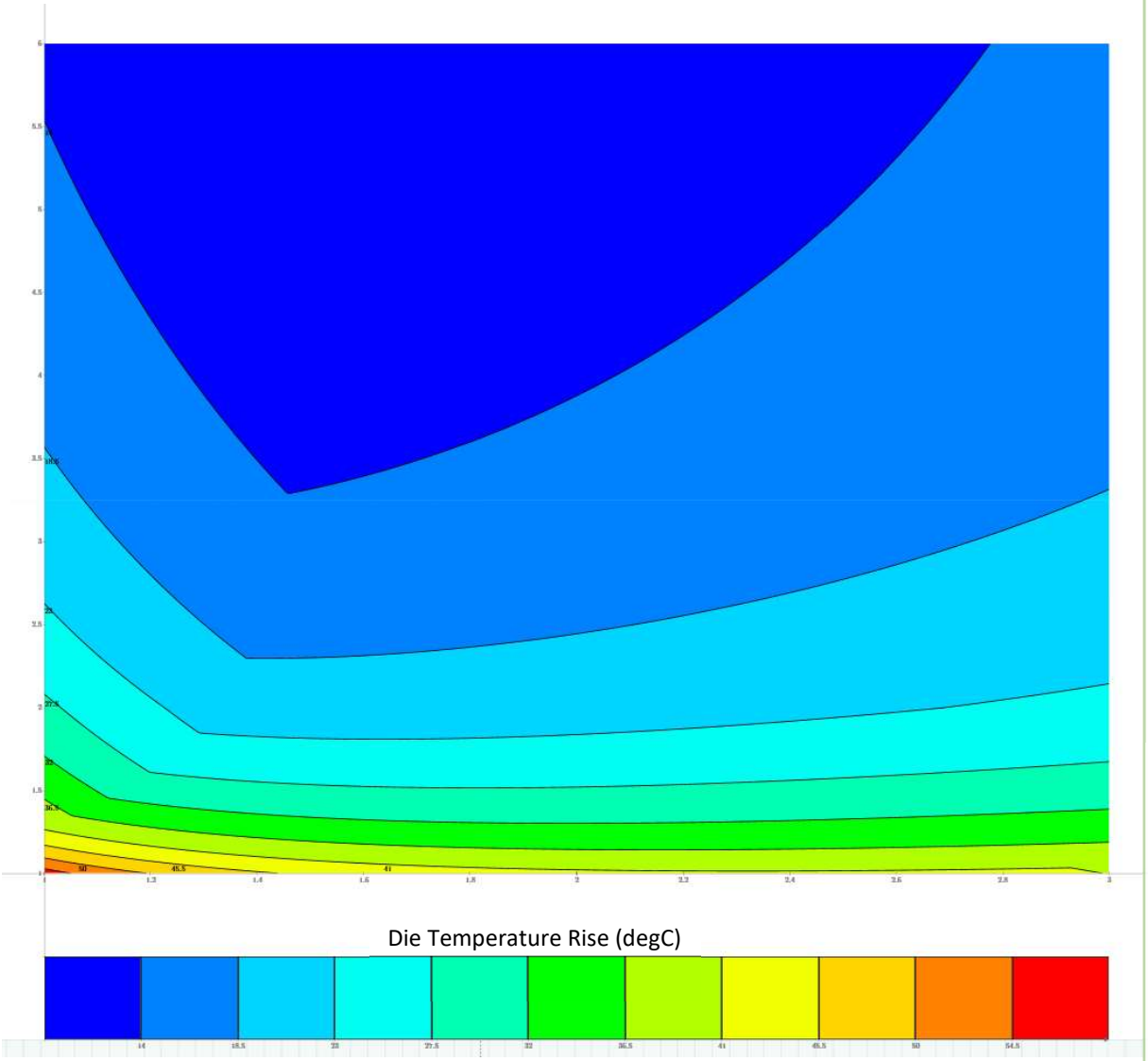
# P1000 TX Application Note 3: Design the Application

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5 October 2022

# P1000 TX Application Circuit Description: Design the Application

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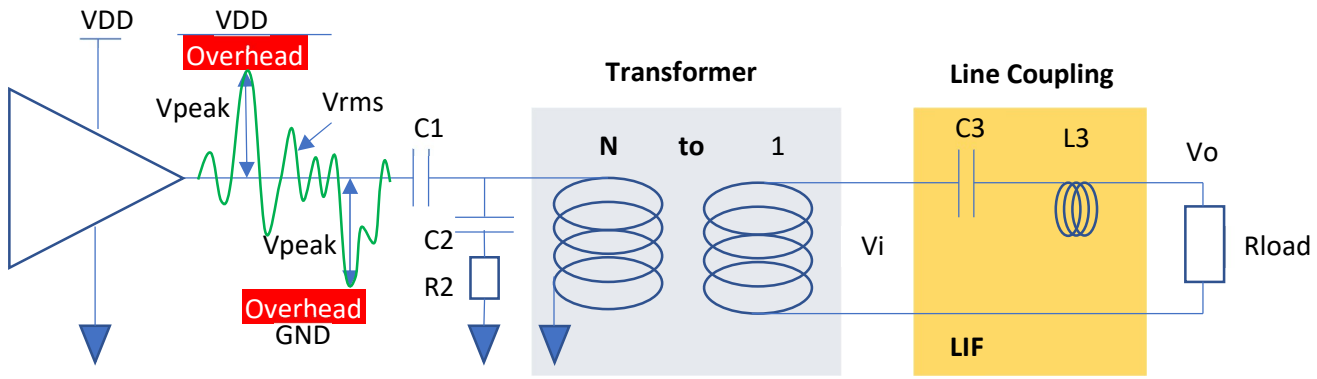
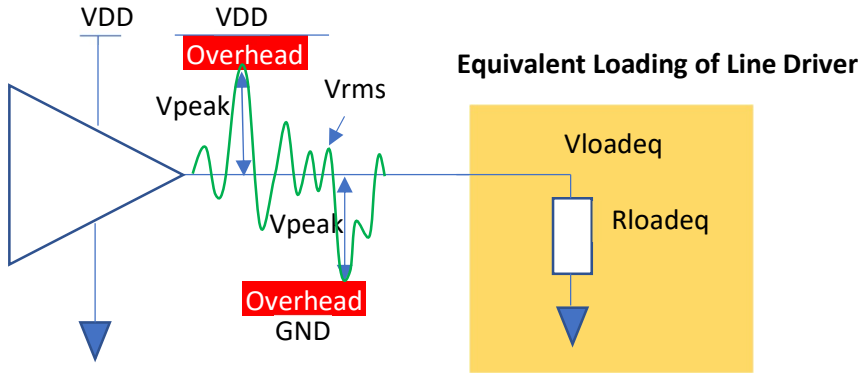
Various parameters can affect the performance of the narrow band Power Line Communications channel. Properly understanding and optimizing these parameters will lead to a high performing, robust system with minimum tradeoffs. This series of application notes will discuss power dissipation, die temperature, and overhead voltage which are crucial for reliable system. The Line Coupling interface application note describes the interface to the line and how to modify and optimize the line interface to minimize the attenuation. The resultant is the LIF factor. The Power Dissipation application note describes the power calculations, the temperature increase calculations, and the overhead voltage requirements. Building upon the previous application notes, this application note describes how to combine the coupling optimization with the ability to calculate the power dissipation to adjust the transformer ratio and VDD to maximize the signal output at a given load while maintain a safe die temperature and current output.

Below is a schematic of the system with the interface circuitry including a transformer coupling. If the entire application circuit was replaced with just an equivalent load it would look like the next picture. This simplified model will make the analysis easier but remember that the Rloadeq depends on the transformer ratio, the Rload, and rest of the components.




Circuit with the equivalent load.



***Calculation of Vloadeq and Rloadeq***

Starting with the previous schematic showing the various cascaded sections of the application circuit, the equivalent values voltage and impedance can be calculated. The optimization goals are to maximize the Vrms signal on the line and minimize the die temperature increase which then maximizes the safe ambient temperature. The application is governed and/or limited by the appliable standards, the line load impedances, and the overhead voltage properties of the line driver. The main variables that can be optimized are VDD and the transformer ratio N. Possible trade-offs in Vo and Rload might be necessary.

Using the definition from the Line Coupling Application Note 1, the LIF or Line Interface Factor is scaler value that represents the total average gain across a frequency varying circuit. The acronym is made up for convenience. Calculated values are shown below in the table.

***LIF Values for various applications***

| *LOAD IN OHMS* | *CELELEC A* | *CELELEC B* | *FCC* |
|---|---|---|---|
| *50* | ***1*** | ***1*** | ***1*** |
| *10* | ***0.97*** | ***1*** | ***1*** |
| *2* | ***0.69*** | ***0.95*** | ***0.95*** |
| *1* | ***0.5*** | ***0.85*** | ***0.85*** |

The equivalent voltage (Vloadeq) needed at the line driver output is shown below, where Vo is the voltage at the load, LIF is defined above, and N is transfer ratio. Other factors could affect the voltage level at the line driver and perhaps could be addressed in the future.

$$Vloadeq = \frac{Vo}{LIF} * N$$

Since the Load current is not shunted by the line coupling LIF circuit, it is the current through the load translated through the transformer as shown here.

$$Iloadeq = \frac{Vo}{Rload} * \frac{1}{N}$$

The equivalent load is Vloadeq divided by Iloadeq, thus it ends up with a squared N and dependent on LIF.

$$Rloadeq = \frac{Rload}{LIF} * N^2$$

***How to calculate the Minimum VDD required***

The VDD needs to large enough to accommodate the overhead voltages and the signal voltage, Vloadeq, and the Crest Factor (CF). However, VDD is limited by the line driver fabrication process and the maximum safe die temperature. The overhead voltages mentioned in previous application note (Power Dissipation Note 2) are limited by various circuit configurations and device sizes. In the P1000, only the device size limits the overhead. The CF is the ratio of the peak voltage to the rms voltage and is discussed in the power dissipation application note.

Since the overhead voltages are dependent on the operating conditions (ID, VDS) of the output devices, a resistor model can be used as simple estimate of what overhead voltage is needed to stay in the saturation region. The P1000 allows 3A drive with 2 Volts of overhead overall process and temperature corners. It also works with 1V at 1.5A, thus the resistor model (Rlinearmodel) is 2/3 Ohms. Using this to calculate the overhead by the following equation:

$$Voverheadlimit = Rlinearmodel * Iloadeq$$

$$Voverhead \geq Rlinearmodel * Iloadeq$$

As written in the previous Application note about power Dissipation, the signal for this application note is considered an OFDM signal with a Crest Factor (CF) which represents the Vpeak to Vrms of the signal. The peak-to-peak signal (2X the peak signal) is

$$Vppeq = Vrmseq * CF * 2$$

Combining all the constraints to form a formula for a minimum VDD voltage as

$$VDDmin = Vppeq + 2 * Voverheadlimit = Vrmseq * CF * 2 + 2 * Rlinearmodel * Iloadeq$$

Substituting earlier definition equations produces the VDDmin equation below

$$VDDmin = \frac{Vo}{LIF} * N * CF * 2 + 2 * (Rlinearmodel) * \frac{Vo * CF}{Rload} * \frac{1}{N}$$

VDD can be larger than VDDmin, but not smaller. If the VDD is chosen much larger than VDDmin, then the power might be higher than if it was exactly VDDmin. If VDD needs to be smaller, adjust Vo, Rload, etc. to achieve the goal. Also, the P1000 has a min and max VDD of 10V and 22V respectively.

Other equations that determine the constraints are the maximum current and maximum die temperature. 3Apeak is considered the minimum maximum current of the P1000. (Confused, it will always be able to drive at least 3Ap)

$$Ichipmax \geq \frac{Vo}{Rload} * \frac{1}{N} * CF$$

Solved in the power dissipation application note for an OFDM signal, the factor relating the IVDDavg to Iloadeqrms is shown below.

$$\frac{IVDDavg}{Iloadeqrms} = 0.4$$

The total power is calculated below from the on-chip power minus the load power.

$$TotalDiePower = VDD\ power - Load\ pwr + Queisent\ power = VDD * \frac{Vo}{Rload} * \frac{1}{N} * 0.4 - \frac{(\frac{Vo * N}{LIF})^2}{Rload} + Pq$$

ThetaJA (degrees C/Watts) is used to represent the rate of temperature change between the die and ambient air including the thermal interfacing between the die, package, and board. Power times Theta JA provides the temperature delta between die and ambient. Pq is the non-output related power of the chip, usually VDD*Iq. Here is the delta temperature calculation.

$$Tempdelta = \left( VDD * \frac{Vo}{Rload} * \frac{1}{N} * 0.4 - \frac{\left(\frac{Vo * N}{LIF}\right)^2}{\frac{Rload}{LIF} * N^2} + Pq \right) * ThetaJA$$

***Calculate Temperature Increase***

There are several ways to setup a series of equations that will calculate the temperature rise, the minimum VDD, and to check if the design exceeds the maximum current and/or minimum overhead voltages.

One way is to implement the above equations in Excel. It is fairly simple to do to the amount of detail desired. Below is a clip of an Excel spreadsheet setup for an FCC signal with various conditions. Often transformer ratios and VDD could be fixed or limited in selection, so this method is an effect way to design the application.



1) Vary parameters below that have orange header blocks to maximize your safe temperature while providing you with extra drive
2) Overhead blocks, Continuous and Short term Temperatures can turn RED (avoid) or Yellow (use caution) when you change the orange values.

Damping Ckt Imped. (Ohms) (i): 10000

Continuous Junction Temp (electromigration): 135

Short Term Junction Temperature (below TSD): 150

| At HV Load Side of XFMR | | | | | | | At LV Line Driver side of XFMR | | | | | | | | | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Vload rms (a) | Rload (b) | Ipeak (using PAR value) | Component transfer V/V (c) | Vout HV side of XFMR | Effective Load on HV side | XFMR ratio N:1 (d) | Vout rms | Effective Rload | Iout rms | Load Pwr Avg | PAR (e) | Vpeak | Ipeak | VDD (f) | Overhead Voltage RED is Vovh/Iout < 2V/3A | VDD Iavg from driving load | Quiesent current (without driver I) | Quiesent Power | Damping Ckt current at Vout | Total VDD Iavg = Load + Quiesent + Damping ckt | Amp Pwr w/ load w/ Quiescent | Final Efficiency | Amp Pwr w/Quiesent + Damping w/o Load | theta JA (g) | Rise in temp | Ambient Temp | Final die temp @ 25C | Max Continuous Ambient Temperature RED <25C, Yellow <85C | Max Ambient Temp for Short Term |
| Vrms | Ohms | Apeak | V/V | Vrms | Ohms | windings | Vrms | Ohms | A rms | Wavg | V/V | Vpeak | Ipeak | V | V | Iavg | Idc | Wavg | Irms | Iavg | Wavg | % | Iavg | degC/W | C | C | C | C | C |
| 1.5 | 10 | 0.53 | 1.00 | 1.50 | 10.00 | 2 | 3.00 | 40.00 | 0.08 | 0.23 | 3.50 | 10.50 | 0.26 | 22 | 0.50 | 0.030 | 0.034 | 0.75 | 0.000 | 0.064 | 1.411 | 16.0 | 1.19 | 17 | 20.2 | 25 | 45.2 | 114.8 | 129.8 |
| 1.31 | 2 | 2.29 | 0.90 | 1.46 | 2.22 | 2 | 2.91 | 8.89 | 0.33 | 0.95 | 3.50 | 10.19 | 1.15 | 22 | 0.81 | 0.131 | 0.034 | 0.75 | 0.000 | 0.165 | 3.633 | 26.2 | 2.68 | 17 | 45.5 | 25 | 70.5 | 89.5 | 104.5 |
| **0.86** | **1** | **3.01** | **0.85** | **1.01** | **1.18** | **1** | **1.01** | **1.18** | **0.86** | **0.87** | **3.50** | **3.54** | 3.01 | **11.1** | 2.01 | **0.344** | **0.034** | **0.38** | **0.000** | **0.378** | **4.196** | **20.7** | **3.33** | 17 | **56.5** | **25** | **81.5** | 78.5 | 93.5 |

The following equations, developed in MathCad, are used to solve for the 1) Maximum current of line driver (Eq 1), 2) Minimum VDD (Eq 2), 3) Temperature increase with minimum VDD (Eq 3), and 4) Temperature increase with fixed VDD (Eq 4). The Temperature rise can be calculated with the minimum VDD by adding the VDD equation reference to the temperature as shown in Eq 3. Also, the LIF can be set up to change according to the load impedance, and conditional statements can be used to limit the VDD minimum to conform to range of 10 to 22V which is the line driver's limits.

Define LIF as a Linear Interpolation function

$$LIFc := \begin{bmatrix} .85 \\ .95 \\ 1 \end{bmatrix} \qquad LIFr := \begin{bmatrix} 1 \\ 2 \\ 10 \end{bmatrix}$$

$$LIF(Rload) := \text{linterp}(LIFr, LIFc, Rload)$$

Define variables and the output voltage at the load, Vo

$$Vo := 0.86 \qquad CF := 3.5 \qquad Rlm := \frac{2}{3} \qquad TJA := 17 \qquad Iq := 34 \cdot 10^{-3}$$

Define functions to calculate, max Chip current and minimum VDD

$$Ichipmax(Vo, N, CF, Rload) := \frac{Vo}{Rload} \cdot \frac{1}{N} \cdot CF$$

Eq 1

$$VDDmin(Vo, N, CF, Rload, Rlm) := \left\| \begin{array}{l} x \leftarrow \frac{Vo}{LIF(Rload)} \cdot N \cdot CF \cdot 2 + 2 \cdot Rlm \cdot \frac{Vo \cdot CF}{Rload} \cdot \frac{1}{N} \\ \text{if } x > 22 \\ \quad \| \, x \leftarrow 22 \\ \text{if } x < 10 \\ \quad \| \, x \leftarrow 10 \\ \text{return } x \end{array} \right.$$

Eq 2

$$Tempdelta(Vo, N, CF, Rload, Rlm, Iq, TJA) := \left( VDDmin(Vo, N, CF, Rload, Rlm) \cdot \left( Iq + \frac{Vo}{Rload} \cdot \frac{1}{N} \cdot 0.4 \right) - \left( \frac{\left( \frac{Vo \cdot N}{LIF(Rload)} \right)^2}{\frac{Rload}{LIF(Rload)} \cdot N^2} \right) \right) \cdot TJA$$

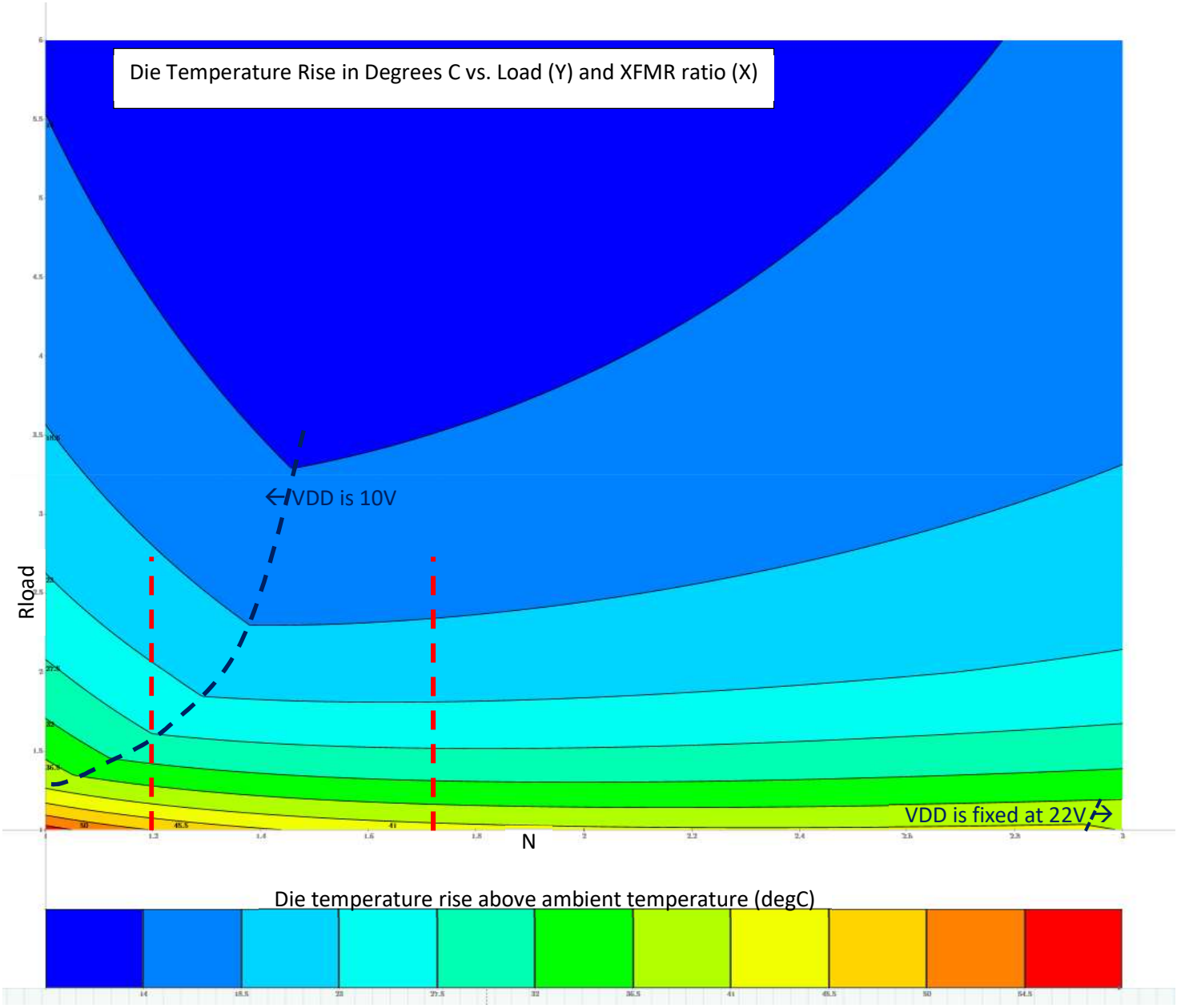
Eq 3

$$TempdeltaVDD(Vo, N, CF, Rload, Rlm, Iq, TJA, VDD) := \left\| \begin{array}{l} vps \leftarrow VDDmin(Vo, N, CF, Rload, Rlm) \\ \text{if } vps \le VDD \\ \quad \| \, x \leftarrow \left( VDD \cdot \left( Iq + \frac{Vo}{Rload} \cdot \frac{1}{N} \cdot 0.4 \right) - \left( \frac{\left( \frac{Vo \cdot N}{LIF(Rload)} \right)^2}{\frac{Rload}{LIF(Rload)} \cdot N^2} \right) \right) \cdot TJA \\ \text{else} \\ \quad \| \, x \leftarrow 0 \\ \text{return } x \end{array} \right.$$

Eq 4

Below is a contour plot where the colors represent the change in temperature, the X axis represents the change in the transformer ratio N, and the Y axis represents the load impedance. The lowest minimum VDD was set to 10V and the maximum VDD allowed is 22V. VDD is calculated to be minimum for a given Vo, CF, etc., however, if this value is less

than 10V, it is forced to 10V, which means the power may go up as shown on the graph to the left of the red dotted curve. If it exceeds 22V it is set to 22V, but it would not be valid since it would have insufficient overhead. From the graph below, the die temperature change is worse at the low ratios and low impedance, but still compliant. The larger the current the more overhead voltage is needed and thus the more on-chip power dissipation. The contour graph shows the influences of both the load and the transformer ratio N. There is a wide range of N values that would provide low die temperature increase if an optimum VDD is chosen. However, the choice may end up being about what VDD voltage is available and/or what various N:1 ratio transformers are available.




To keep a safe temperature limit of 135C long term, 150C short term with an ambient temperature of 85C, means-

135C – 85C= 50C is the maximum die temperature rise.
150C – 85C= 65C is the short-term max die temp. rise.

From the above contour plot, two N values are chosen to illustrate how to use the graph. The two red dashed lines represent a constant N=1.2 and N=2. The values of die temperature change are grouped in color coded bands. As the reader can see, dotted lines cross more moderate temperature change bands which is what desired. If the low impedance drive is not necessary or only low VDD's are available, a place on the graph could most likely be found to help determine a solution for those requirements. Using Equations 3 and 2, to calculate the temperature change and minimum VDD for various loads, the results are shown below.

***Die Temperature Rise vs. Loads and VDD for N=1.2 example***

| *LOAD IN OHMS* | *VDD MIN* | *TEMP INCREASE* |
|---|---|---|
| *1* | ***11.8V*** | ***49.8C*** |
| *1.5* | ***10.3V*** | ***29.9C*** |
| *2* | ***10V*** | ***23.5C*** |
| *5* | ***10V*** | ***12.9C*** |

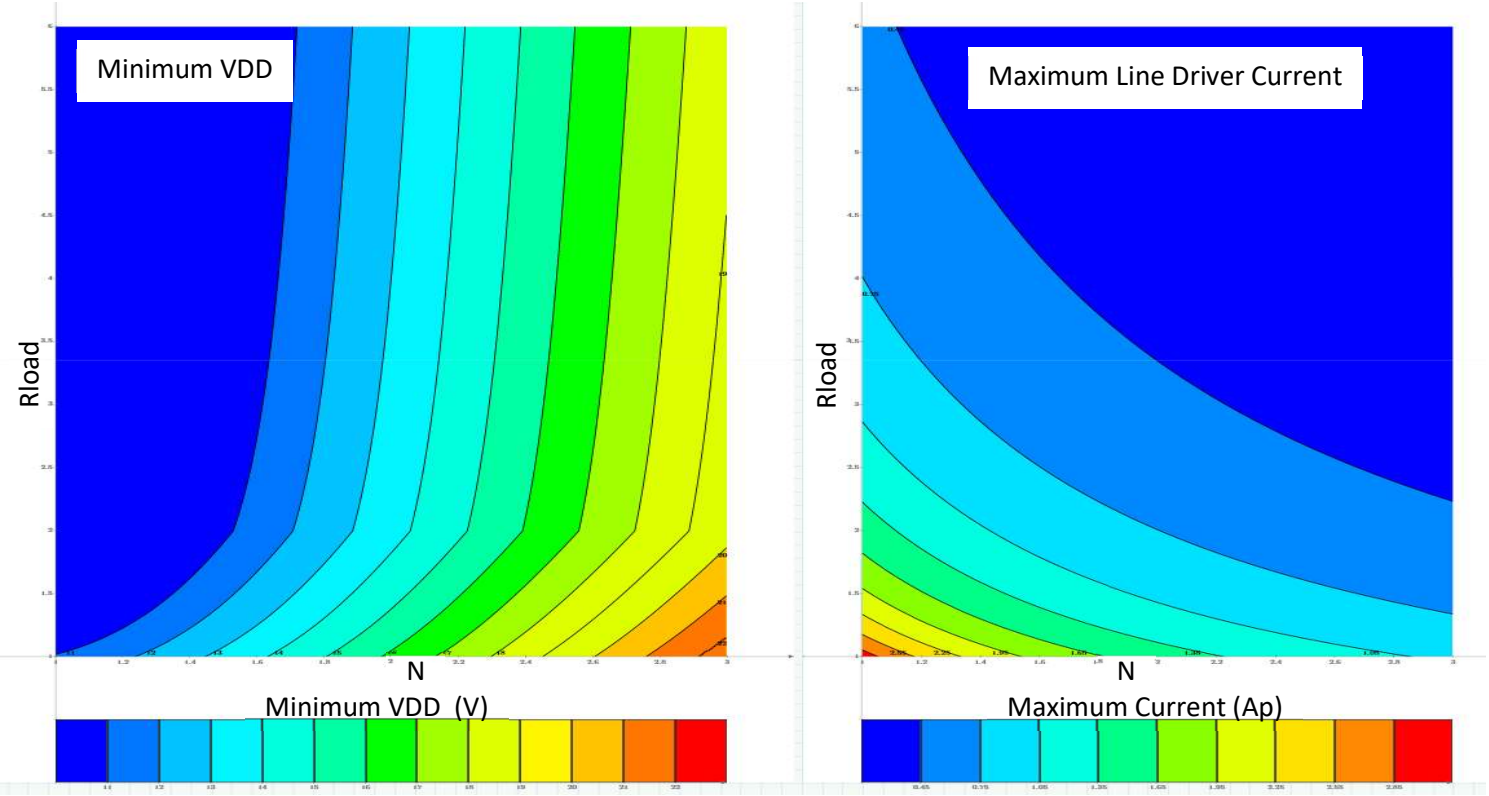
***Die Temperature Rise vs. Loads and VDD for N=2 example***

| *LOAD IN OHMS* | *VDD MIN* | *TEMP INCREASE* |
|---|---|---|
| *1* | ***16.2V*** | ***41.8C*** |
| *1.5* | ***14.7V*** | ***27.9C*** |
| *2* | ***13.7V*** | ***21.3C*** |
| *5* | ***12.8V*** | ***12.3C*** |

Both examples are within the safe ranges. The minimum VDD is determined by the lowest impedance load case, so for N=1.2, VDD should be set to 11.8V or greater, and for N=2, VDD should be set to 16.2V or greater. This means the power dissipation will go up more than what is in the table (but not to exceed the 1 Ohm temperature change) for the higher impedance loads, which should not be an issue.

The graphs below show the Minimum VDD (left) and Maximum line driver current (right). On the Minimum VDD graph, the bend as it approaches low impedance loads is mostly due to the LIF being load impedance dependent and thus the need for a greater VDD to accommodate the larger voltage signal out of the line driver (because LIF is getting smaller) at low impedance loads.

The maximum current appears at the N near 1 and Rload near 1 Ohm. If the output voltage goal is too high or the transformer ratio is too low, this graph will illustrate the possible occurrence of an over current condition. The maximum current of the P1000 is 3Ap and there are four setting for the current limiter (3.1A, 2.7A. 2.1A, 1.7A). Once the output current exceeds this preset limit, the output will clip to prevent the current from increasing beyond that limit. Choosing the short circuit limit depends on the "N" ratio and what maximum current is shown in this graph. To lower the changes of the line driver overheating, the short circuit setting should be chosen close to the maximum current level of the applicable application. It should be high enough to guarantee that it does not interfere with normal operation while additionally accounting for normal variations of parameters.



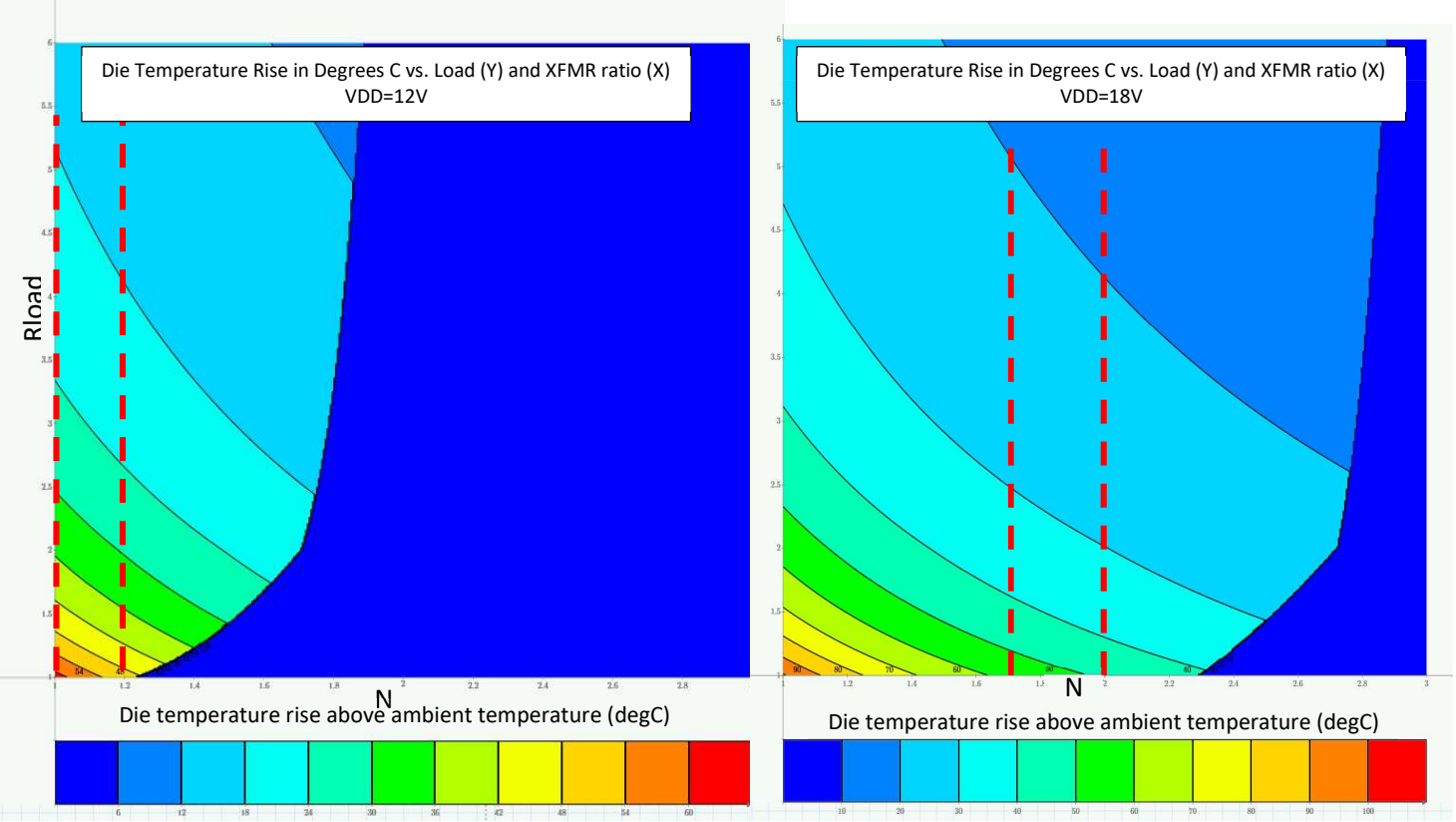

***Fixed VDD, Die Temperature Rise***

In the cases where VDD voltage is already established and the line interface must be optimized to this value, Equation 4 is helpful because VDD is an input. With the other assumptions of Vo=0.86Vrms, CF=3.5, Rload as low as 1 Ohm, two graphs were developed below, one for VDD=12V and the other for VDD=18V. The dark blue shows where the calculated Minimum VDD is greater than the input VDD and thus is not a valid design space.

The left graph below shows a fixed VDD=12V. The graph shows that an "N" value between 1-1.2 is possible with a VDD=12V. The results from the VDD=12V calculations are shown in the below table. At 1 Ohm and 1:1 ratio, the rise in temperature just lower than the 150C short term limit for 85C. If this is too close, perhaps consider dropping the VDD to 11.2V if possible. Otherwise, both this will work for 12V case.

***Die Temperature Rise vs. Loads and Ratio of Transformer for VDD=12V (50C max for 135C, 65C max for 150C)***

| *LOAD IN OHMS* | *VDD* | *1:1* | *1.2:1* | *COMMENT* |
|---|---|---|---|---|
| *1* | ***12V*** | ***62.3*** | ***50.6*** | ***Close with 1:1**** |
| *1* | ***11.2V*** | ***57.2*** | | ***Better VDD choice*** |
| *1.5* | ***12V*** | ***44.4*** | ***39.7*** | ***Ok with both*** |
| *2* | ***12V*** | ***35.4*** | ***32*** | ***Ok with both*** |
| *5* | ***12V*** | ***18.4*** | ***17*** | ***Ok with both*** |




At VDD=18V, the ratios are moved up to 1.68 and 2 as shown on the above graph (right side). At 18V the 1.68:1 ratio transformer application has a higher die temperature rise and the 1 Ohm case only qualifies for the 150C die temperature limit. If VDD=15V is possible, it is a better choice for 1 Ohm with only 46C rise instead to 58C and will work with the 135C die temperature limit. But if given only an 18V supply, 2:1 is a good choice since it has a low temperature change and is compliant with both limits.

***Die Temperature Rise vs. Loads and Ratio of Transformer for VDD=18V example***

| *LOAD IN OHMS* | *VDD* | *1.68:1* | *2:1* | *COMMENT* |
|---|---|---|---|---|
| *1* | ***18V*** | ***58.3*** | ***48.2*** | ***Close for 1.68*** |
| *1* | ***15V*** | ***46.1*** | | ***Better VDD choice*** |
| *1.5* | ***18V*** | ***42.9*** | ***38.6*** | ***Ok with both*** |
| *2* | ***18V*** | ***35.1*** | ***30.1*** | ***Ok with both*** |
| *5* | ***18V*** | ***21.5*** | ***19.1*** | ***Ok with both*** |

## *Conclusion*

This is a tool to help the designer determine tradeoffs of the line interface application circuit. VDD, N, LIF, Theta JA, etc. all determine the die temperature rise. Optimizing the various variables to provide the necessary line signal (Vo) with the lowest VDD to minimize the power and die temperature increase. Remember that VDD, signals, component values, etc. all vary, so be sure to design your application over the range of variations. Leaving margin is also a good idea where possible and will improve the changes of it working robustly in real world situations. The board layout also makes a huge difference to the ThetaJA, design it well. Simulate your circuit, if available. Thus, the information from these three applications notes should assist the reader's understanding of the tradeoff relationships necessary to design a reasonable, compliant TX line driver application circuit. If you need help, contact me at info@plan9inc.com.