Plan 9 is offering a Thermal Shutdown (TSD) and Reference IP block to complement its other narrow band PLC IP. The TSD shuts down the transmitter when the temperature exceeds the setpoint. The reference provides low variation bias currents to the TX and Rx using a single off-chip resistor.

Applications include:

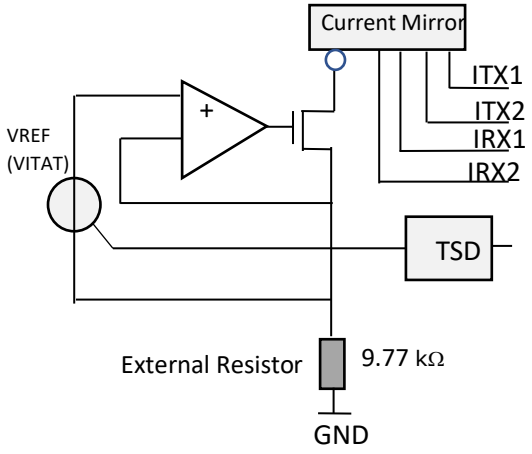
- *All PLC related standards*
- *Smart power meter communications*
- *Smart House controls*
- *Industrial Internet of Things*

Features of this TSD Reference IP:

- *1 mA operating current*
- *Generation of all RX and TX bias currents using a single off-chip resistor*
- *6ppm/˚C Temperature independent voltage from -40 to 150 ˚C.*
- *Thermal shutdown (TSD) @ 158˚C with 15˚C Hysteresis*
- *Power down mode w/ low idle current*
- *IP cell area is 0.204mm^2*

Description

The reference is comprised of a temperature independent voltage reference, a GM stage (using a single off-chip precision resistor) and a current distribution network. A thermal shutdown is implemented based on the difference between the voltage reference and a diode voltage.

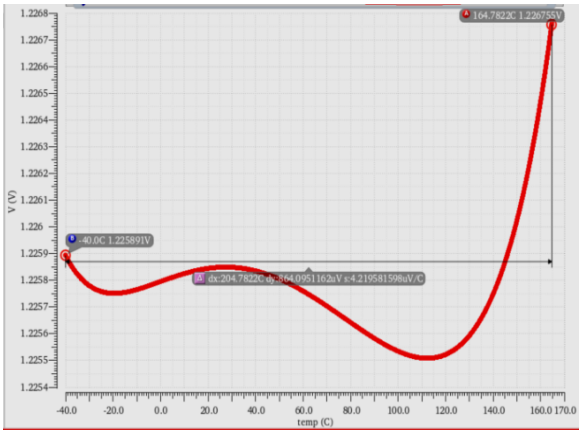


Performance:

Temperature independent voltage reference, ± 3% variation over process.

TX and RX bias currents 6% variation with single off-chip 5% resistor.

Thermal shutdown at 158 ˚C ± 5˚C A 15 ˚C hysteresis allows IC cooling before recovery.



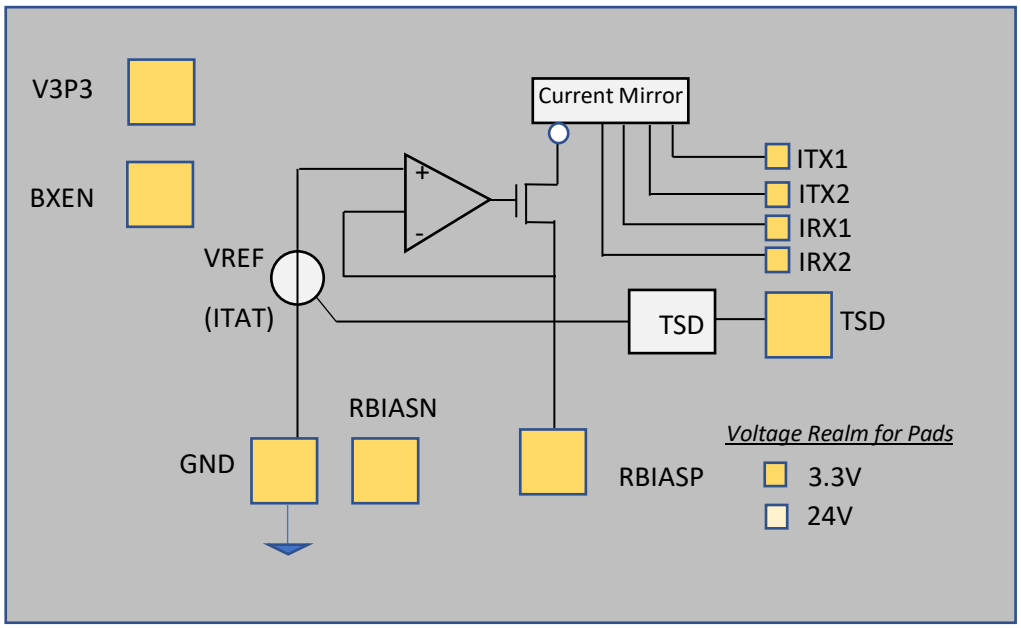
Reference Voltage vs. Temp

Availability

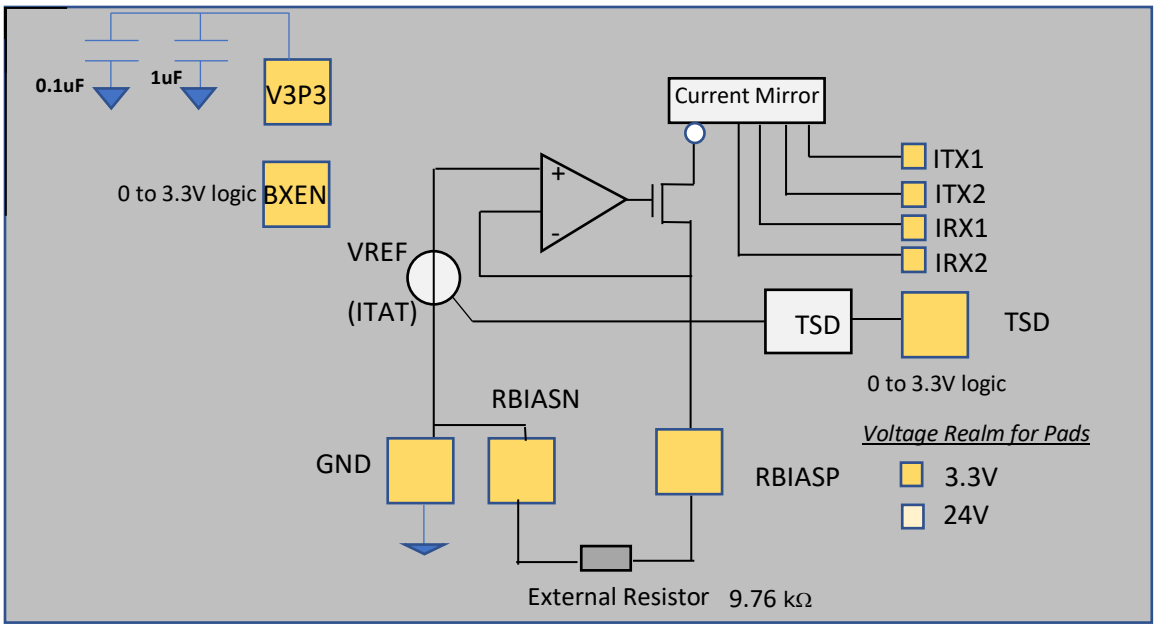
Additional information and demos are available with restrictions. Email: info@plan9inc.com

The IP ownership is offered for sale.

Block Diagram



Application Circuit



Pin Description

Pin Name	Pin on Package	ESD Requirements	Description
V3P3	24	5V	Receiver Supply voltage typically 3.3 V ±10%
BXEN	28	5V	Active Bias from standby, H-active
RBIASN	27	5V	Negative external resistor connection
RBIASP	26	5V	Positive external resistor connection
GND	Paddle	none	Down bonded to package paddle
ITX1	Internal	5V	Low variation bias current, 500 µA Main TX
ITX2	Internal	5V	Low variation bias current, 128 µA Auxiliary TX
IRX1	Internal	5V	Low variation bias current, 20 µAPGA1
IRX2	Internal	5V	Low variation bias current, 20 µA PGA2
TSD	19	5V	Thermal Shutdown, H-active

Specifications

Simulation results are included to show how well the silicon matches simulation. Agreement between measured and simulated values validates the simulations and that layout minimally impacts the design. Thus, with good agreement, simulations over the corners can be more relied upon to help predict long term manufacturing performance limits.

Below are the Overall Conditions for testing, except where noted. The TSD Reference was tested over combinations of voltage, temperature, and process corner. In addition, Monte Carlo analysis was employed for certain tests.

Corners used are Typ., FF, SS, FS, SF with various combinations of resistor and capacitor corners.
VDD = 10V and 24V (tested at extreme range, see recommendations)
V3P3 = 3V,3.3V and 3.6V
Junction Temperature = -40C, 27C, and 150C
Rload= 1M Ω (resistive load)
Cload= 20pF

Absolute Max

Symbol	Description	Conditions	Min	Typ	Max	Units
	V3P3 Supply Range		-0.4		5.5	V
	BXEN, TSD, RBIASP, RBIASN		-0.4		5.5	V
	Junction Temperature		-40		150	C

Recommended

Symbol	Description	Conditions	Min	Typ	Max	Units
	V3P3 Supply Range		3		3.6	V
	Junction Temperature		-40		135	C

Power Supply Voltages and Currents

			Spec/Sim			Measured			
Symbol	Description	Conditions	Min	Typ	Max	Min	Typ	Max	Units
	V3P3 Supply Range		3	3.3	3.6	3	3.3	3.6	V
	Bias V3p3 Active Current	No signal (includes Plan 9 bias)		828			689		µA
	Bias V3P3 Powered Down Current		8		42				nA

Reference Voltage and Currents

			Spec/Sim			Measured			
Symbol	**Description**	**Conditions**	**Min**	**Typ**	**Max**	**Min**	**Typ**	**Max**	**Units**
	Start time	V3P3=3.3V		765					ns
	VREF	V3P3=3.3V		1.225			1.2097		V
	ITX1	V3P3=3.3V		500			504		µA
	ITX2	V3P3=3.3V		128			120		µA
	IRX1	V3P3=3.3V		20			18		µA
	IRX2	V3P3=3.3V		20			18		µA
	TSD Setpoint	V3P3=3.3V	152	158	168		160		°C
	TSD Hysteresis	V3P3=3.3V		14			10		°C

Physical

Cell Dimensions : X 228 µm Y 896 µm

Cell Area 204288 μm^2